

PTO/SB/33 (07-05)

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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) IMPJ-0003D1 (033327-056)		
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for	Application Number 10/661,037		Filed 09/12/2003	
Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on 11/22/2006	First Named Inventor John D. Hyde			
Typed or printed Name Julie Arango	Art Unit 2822		Examiner Soward, Ida M.	
Applicant requests review of the final rejection in the above-ider with this request.	ntified applica	tion. No ame	endme	nts are being filed
This request is being filed with a notice of appeal.				
The review is requested for the reason(s) stated on the attached Note: No more than five (5) pages may be provided.	d sheet(s).			
I am the	_WA		Signatu	re
applicant/inventor. assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)	Khaled S	Shami Typed or	printed	name
attorney or agent of record. Registration number	408-2	92-5800	phono	number
attorney or agent acting under 37 CFR 1.34. Registration number 38,745	11/22/		phone r	iumbei
			Date	
*Total of 1 forms are submitted.				

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:

John D. Hyde et al.

CONFIRMATION NO.: 6704

SERIAL NO.:

10/661,037

FILING DATE:

09/12/2003

TITLE:

pFET SYNAPSE TRANSISTOR WITH STRUCTURE FOR

FACILITATING CHARGE INJECTION AND/OR TUNNELING WITH

RESPECT TO A FLOATING GATE

EXAMINER:

Soward, Ida M.

ART UNIT:

2822

CERTIFICATE OF MAILING

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Date: 11/22/2006

Mail Stop AF **Commissioner for Patents** P.O. Box 1450 Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Applicant respectfully requests a formal review of the legal and factual basis of the rejections in the above referenced application in view of the following remarks:

The final Office Action fails to account for all the elements recited in the claims. For 1. example. Claim 36 recites first and second n- wells. The final Office Action points to Bergemont's n- well 205 as the second n- well, and to the n- well to the left of that (presumably

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203) as the first n- well. However, Claim 36 also recites first and second p+ regions in the first n- well and third and fourth p+ regions in the second n- well. Bergemont shows p+ regions in second n- well 205, but does NOT show any p+ regions in the n- well to the left of that (that is, n- well 203). Bergemont also does not show other claimed features *relating to the first n- well* (203), such as a channel between a source and a drain, a source contact terminal, and a drain contact terminal. While similar features are shown in relation to the second n- well 205 of Bergemont, none are show in relation to the first n- well (203) as Claim 36 expressly and clearly recites. Bergemont also fails to teach recited features in other claims, which the Yamashita also fails to teach, and the final Office Action does not address these deficiencies.

2. Bergemont and Yamashita are not properly combinable because their teachings are incompatible. The final Office Action mischaracterizes Applicant's basis for this assertion as advocacy of product-by-process claims. In fact there are no process steps recited in any of Applicant's claims and therefore none of them fall into the class of product-by-process claims. Applicant simply reasoned that the teachings of Bergemont and Yamashita are incompatible because they employ processes that are inconsistent with each other and with their stated goals to achieve products that are also different and incompatible. Bergemont is directed to EEPROM memories, which operate on electron tunneling principals, primarily through gate oxides. Conditions required to permit tunneling are very specific and impose strict limitations on operational, material and dimensional parameters. In addition, the object of Bergemont is to realize a device that can be fabricated consistent with CMOS processing procedures. Otherwise EEPROM devices can only be economically produced in bulk, and cannot be efficiently incorporated into SOC (system-on-chip) devices as Bergemont seeks to do. Yamashita, by

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comparison, is not concerned with CMOS processing and introduces numerous fabrication steps that are inconsistent with CMOS processing and would add tremendous costs to the fabrication, in direct contravention of the stated goals of Bergemont. It was this argument against the combination of Bergemont and Yamashita that Applicant advanced and that the final Office Action mischaracterized as an argument for the patentability of product-by-process claims, when in fact no such claims are present in the instant application.

Please charge any additional required fees, or credit any overpayment to our deposit account no. 50-1698.

Respectfully submitted,
THELEN REID & PRIEST, L.L.P.

Dated: <u>11/22/2006</u>

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